(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
15 January 2004 (15.01.2004)

PCT

(10) International Publication Number
WO 2004/006440 A1

(51) International Patent Classification[7]: H03M 3/00, 1/66

(21) International Application Number:
PCT/US2003/011777

(22) International Filing Date: 16 April 2003 (16.04.2003)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
10/191,016 8 July 2002 (08.07.2002) US

(71) Applicant: CIRRUS LOGIC, INC. [US/US]; 2901 Via Fortuna, Austin, Texas 78746 (US).

(72) Inventor: MELANSON, John, Laurence; 901 West 9th Street, #201, Austin, TX 78703 (US).

(74) Agent: MURPHY, James, L.; Winstead Sechrest & Minick P.C., P.O.Box 50784, 1201 Main Street, Dallas, TX 75250-0784 (US).

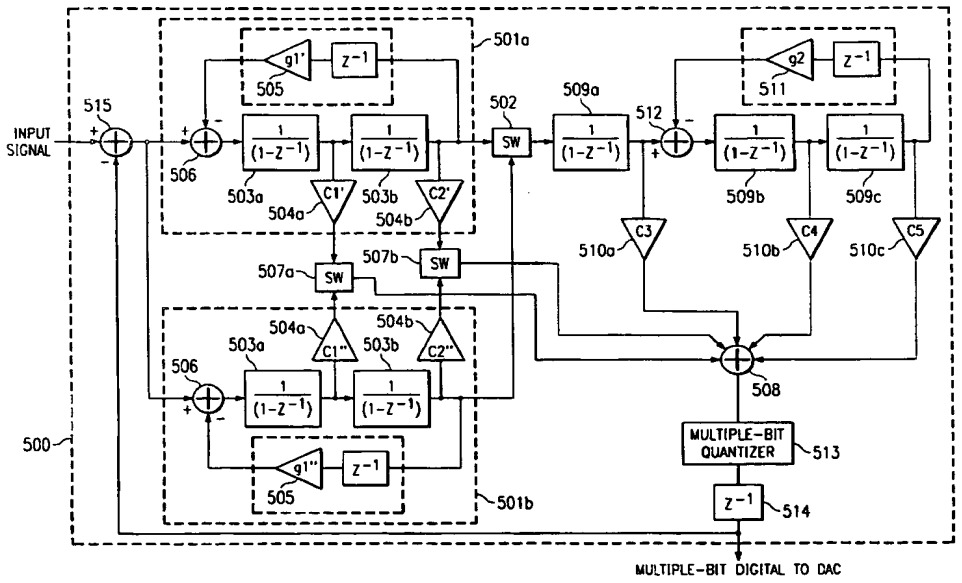
(81) Designated States (national): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States (regional): ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: DELTA-SIGMA MODULATION CIRCUITS AND METHODS UTILIZING MULTIPLE NOISE ATTENUATION BANDS AND DATA CONVERTERS USING THE SAME



(57) Abstract: A noise shaper including a filter system (501a, 50b) for generating a first set of poles and zeros characterizing noise attenuation in a signal baseband of a noise transfer function and at least one additional set of at least one pole and one zero characterizing noise attenuation in at least one additional band outside the baseband of the noise transfer function.

WO 2004/006440 A1

DELTA-SIGMA MODULATION CIRCUITS AND METHODS UTILIZING MULTIPLE NOISE ATTENUATION BANDS AND DATA CONVERTERS USING THE SAME

BACKGROUND OF THE INVENTION

FIELD OF INVENTION

The present invention relates in general to delta sigma modulators and in particular, to delta-sigma modulation circuits and methods utilizing multiple noise attenuation bands and data converters using the same.

BACKGROUND OF INVENTION

Delta-sigma modulators are particularly useful in digital to analog and analog to digital converters (DACs and ADCs). Using oversampling, the delta-sigma modulator spreads the quantization noise power across the oversampling frequency band, which is typically much greater than the input signal bandwidth. Additionally, the delta sigma modulator performs noise shaping by acting as a lowpass filter to the input signal and a highpass filter to the noise; most of the quantization noise power is thereby shifted out of the signal band.

The typical delta sigma modulator includes a summer summing the input signal with negative feedback, a linear filter, quantizer and a feedback loop coupling the quantizer output and the inverting input of the summer. In a first order modulator, the linear filter comprises a single integrator or other filter stage while the loop filter in a higher order modulator comprises a cascade of a corresponding number of filter stages. Higher-order modulators have improved quantization noise transfer characteristics over those of lower order, but stability becomes a more critical design factor as the order increases. The quantizer can be either a one-bit or a multiple-bit quantizer.

Switched-capacitor filters / integrators are useful in a number of applications including the integrator stages in delta sigma modulators. Generally, a basic differential switched-capacitor integrator samples the input signal onto sampling capacitors during the sampling (charging) phase. A reference voltage may also be sampled onto a reference sampling capacitor during this phase to implement a

DAC function in the feedback loop of an ADC. During the following dump phase, the charge on the sampling capacitor is transferred to the summing node of an operational amplifier and an integrator capacitor in the amplifier feedback loop. The operational amplifier drives the integrator output.

One drawback with switched-capacitor filters, and similar circuits, such as current steering DACs operating in multiple phases, is inefficiency. In the case of a switched-capacitor integrator, the current drive capability of the operational amplifier is only exploited approximately half of the time for a two-phase design. In other words, while the operational amplifier does provide current drive during the dump phase, its current drive capability is generally not used during the sampling phase.

Addressing the problem of circuit inefficiency is major effort, especially in delta-sigma modulator applications. Among other things, an improvement in circuit efficiency can result in a tradeoff of other performance parameters, such as noise attenuation. Hence, some improved techniques are required for designing and constructing efficient multiple-phase filters and associated delta-sigma modulators that do not sacrifice noise performance or other operating characteristics.

SUMMARY OF INVENTION

The principles of the present invention are embodied in circuits and methods for performing delta-sigma modulation with multiple attenuation bands in the noise transfer function. According to one particular embodiment, a noise shaper is disclosed which includes a filter system for generating a first set of poles and zeros characterizing noise attenuation in a signal baseband of a noise transfer function and at least one additional set of at least one pole one and zero characterizing noise attenuation in at least one additional band outside the baseband of the noise transfer function.

Multiple attenuation bands in the delta-sigma modulator noise transfer function realize significant advantages. For example, a delta-sigma modulator with n number of attenuation bands defined on the unit circle in the z-plane will allow an output signal to be interleaved into n number of conversion elements. The noise attenuation in the multiple attenuation bands ensures that noise, which would

otherwise be demodulated by mismatches between the interleaved conversion elements, is minimized. In the case of a switched-capacitor DAC or summer, interleaved conversion elements in turn allow the current capability of the output operational amplifier to be fully exploited in n number of non-overlapping phases. In a current steering circuit, such as a current steering DAC, interleaved current steering elements provide for the generation of a smoother output signal.

BRIEF DESCRIPTION OF DRAWINGS

For a more complete understanding of the present invention, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

FIGURE 1 is a high level functional block diagram of an exemplary digital to analog converter utilizing a delta-sigma modulator with multiple attenuation bands and interleaved conversion elements according to the inventive principles;

FIGURE 2A is a gain versus frequency plot of the noise transfer function (NTF) of an exemplary delta-sigma modulator with two noise attenuation bands;

FIGURE 2B is a plot in the z-plane of the poles and zeros of delta-sigma modulator with multiple NTF noise attenuation bands similar to those shown in FIGURE 2A;

FIGURE 3A is a functional block diagram of a feedforward delta-sigma modulator suitable for producing the pole-zero locations shown in FIGURE 2B;

FIGURE 3B- 3D are gain versus frequency plots of the noise transfer function of the modulator of FIGURE 3A for an exemplary set of feedforward coefficients;

FIGURE 4A is a functional block diagram of a feedback delta-sigma modulator producing asymmetrical sets of pole-zero pairs in the left and right halves of the z-plane;

FIGURE 4B – 4D are gain versus frequency plots of the noise transfer function of the modulator of FIGURE 4A for an exemplary set of coefficients;

FIGURE 5A is a functional block diagram of a delta-sigma modulator with interleave filter stages suitable for generating an NTF with multiple noise attenuation bands;

FIGURE 5B is a pole-zero plot in z-plane illustrating the operation of the modulator of FIGURE 5A;

FIGURE 6 is an electrical schematic diagram of an exemplary DAC with interleaved conversion elements suitable for use in the system of FIGURE 1;

FIGURE 7 is a functional block diagram of a generalized DAC operating in N number of phases in N sets of interleaved conversion elements;

FIGURE 8A is a gain versus frequency plot of the NTF of an exemplary delta-sigma modulator with four (4) noise attenuation bands; and

FIGURE 8B is a pole-zero plot in the z-plane characterizing one possible set of poles and zeros suitable for achieving the NTF of FIGURE 8A.

DETAILED DESCRIPTION OF THE INVENTION

The principles of the present invention and their advantages are best understood by referring to the illustrated embodiment depicted in FIGURES 1 – 8 of the drawings, in which like numbers designate like parts.

Figure 1 is a high-level functional block diagram of a digital to analog converter system 100 suitable for demonstrating the principles of the present invention. For purposes of discussion, an audio application is described operating on digital audio from a source 101 such as a compact disk (CD) or digital versatile disk (DVD) player. Notwithstanding, the concepts described below can be utilized in a wide range of digital to analog, as well as analog to digital, applications.

System 100 is based on a multiple-bit noise shaper 102 with multiple attenuation bands in the noise transfer function (NTF). Noise shaper 102 will be discussed in detail further below; however, generally the NTF includes one attenuation band for attenuating noise in the signal passband and a second attenuation band for attenuating element mismatch noise demodulated by the subsequent splitting of the noise shaper output stream into odd and even samples.

The split into odd and even samples is performed in block 103 which switches the even samples into first dynamic element matching block (DEM 0) 104 and the odd samples into second dynamic element matching block (DEM 1) 105. The outputs from DEM blocks 104 and 105 are respectively passed to even elements 106 and odd elements 107 of DAC 108. DEM blocks 104 and 105 generally reduce mismatch noise by distributing the split output streams from noise

shaper 102 between the individual elements of even and odd element blocks 106 and 107. Two exemplary structures for DAC 108 are described below. Generally, DAC 108 may be either of a switched-capacitor design or a current steering design. In the case of a switched-capacitor design, even and odd elements 106 and 107 will generally comprise switches and sampling capacitors. For a current steering design, even and odd elements 106 and 107 will generally comprise sets of weighted current sources.

Conceptually, during phase Phi 1, switching circuitry shown generally at 112 in FIGURE 1 switches charge or current from even elements 106 to the summing nodes of an output stage 109, represented in FIGURE 1 by a single-ended integrator. At the same time, the inputs to odd elements 107 are sampling the output from DEM 105. During phase Phi 2, the operations are reversed, with even elements 106 sampling the outputs from DEM 104 and odd elements 107 dumping charge or current to the summing nodes at the inputs of output stage 109.

Often, circuits operating in multiple phases, such as switched-capacitor circuits, are not exploited to their full capability. Consider a conventional differential switched-capacitor DAC. During the sampling phase, the differential signals at the DAC inputs are sampled onto a set of sampling capacitors. The charges on the sampling capacitors are then transferred to the differential summing nodes of an operational amplifier integrator during the integration (dump) phase. The operational amplifier provides the current drive to the next circuit block in the system. At the start of the next sampling phase, the summing nodes are decoupled from the sampling capacitors and the process repeats for the next sample. Consequently, while the operational amplifier is active, it is only effectively providing current drive fifty-percent of the time, namely in the integration phase.

It would be desirable to alternate sets of DAC elements or some other technique to fully exploit the current drive capability of the DAC opamps during all operating phases and thereby increase overall system efficiency. For example, one possible technique for increasing efficiency of circuit usage is to independently sample and integrate odd and even samples in alternate phases. In this case, the current drive of the DAC operational amplifier would be utilized almost all of the time. However, the use of alternating DAC elements, normally presents another set of problems.

In one approach, the incoming digital data stream could be modulated in a single delta-sigma modulator and the modulated data split into odd and even samples. The odd and even samples would then be respectively passed through a corresponding odd an even sets of DAC elements, and the resulting odd and even analog signals summed in alternating phases in the DAC opamps. The use of a single delta-sigma modulator has the advantage of achieving good global noise shaping; however, any mismatch between the two separate sets of DAC elements operating on alternating sample streams will demodulate the modulator output noise at the Nyquist frequency (Fs/2). This mismatch-demodulated noise can fold back into the signal baseband.

A second approach is to use two independent delta –sigma modulators for the odd and even data streams and independent DAC elements at the output of each modulator. This technique reduces the problem of potential mismatch demodulated noise between the DAC elements; however, since each delta-sigma modulator is operating on data at half the sampling rate, the global noise shaping function of each NTF is adversely impacted. (Generally, by halving the sample rate through each modulator, the potential noise attenuation in the corresponding signal band is approximately halved.)

In the system of FIGURE 1, the NTF of noise shaper 102 that is selected has at least two noise attenuation bands as shown in FIGURE 2A. This configuration advantageously balances the two approaches discussed above. The low frequency attenuation band attenuates the noise in the signal band and the second band attenuates noise which could be demodulated at the Nyquist rate Fs/2 by splitting (alternating) data streams into separate sets of DAC element 106 and 107 with non-zero mismatch (imperfect matching). In particular, the difference between the average level of attenuation in the signal band and the average level attenuation at Nyquist is a function of the mismatch between even and odd elements 106 and 107 after dynamic element matching. If more mismatch exits, then more modulator noise at Nyquist will be demodulated and therefore more attenuation in the NTF at Nyquist will be required. An increase in attenuation at Nyquist will result in a decrease in attenuation in the signal band. (Generally, the area below the x-axis of FIGURE 2A must equal the area above the x-axis.) Thus, a balancing must be made between the global noise shaping of the NTF and local

attenuation levels. For a one-percent mismatch, a difference in attenuation levels in the signal band and at Nyquist of approximately –40 dB is optimal.

To produce an NTF in noise shaper 102 with a given difference between the average attenuation level in the signal band and the average attenuation at Nyquist, a configuration should be selected with two unequal sets of poles in the left and right halves of the z-plane. A z-plane plot of the pole and zeros characterizing one such noise shaper is shown in FIGURE 2B. In this example, a 6^{th} order noise shaper is characterized which includes a first set of pole-zero pairs 201 that define the shape of the low frequency (signal band) noise attenuation of the NTF. A second set of poles 202 defines the shape of the noise attenuation band at Nyquist. The number of poles and zeros can vary between embodiments, so long as the number of pole-zero pairs around the Nyquist frequency (Re = -1, Im = 0) is less than the number of pole-zero pairs around the DC point (Re =1, Im = 0). In other words, the two sets of pole – zero pairs 201 and 202 are not mirror images. Moreover, a number of different pole - zero placements are possible depending on the desired global and local noise shaping functions. For example, an alternate asymmetrical zero-pole placement would be a single zero at z = -1 and an associated pole on the negative real axis within the unit circuit and two or more zeros on the unit circuit about the DC point and an associated poles within the unit circle.

FIGURE 3A is an exemplary 6th order weighted-feedforward delta-sigma modulator 300 which will produce the zero-pole locations of FIGURE 2B and the corresponding NTF of FIGURE 2A. Modulator 300 generally includes an input summer 301 and a loop filter having four (4) filter stages 302a – 302d each with a response of $1 / (1 - Z^{-1})$ and two (2) filter stages 303a and 303b each with a response of $1 / (1 + Z^{-1})$. The feedforward coefficients Cx are implemented by feedforward stages 304a – 304d, which could be attenuators, amplifiers (gain stages) or multipliers in digital embodiments, driving an output summer 305 from the outputs of filter stages 302a – 302d and 303a – 303b. The output from modulator 300 is generated by a multiple-bit quantizer 306 and a delay element 309 which is also fed-back to the inverting input of input summer 301. The illustrated embodiment also includes three feedback loops 307a – 307c and their respective summers 308a – 308c. A general discussion of delta-sigma modulator

topologies, including feedforward designs, can be found in publications such as, in Norsworthy et al., *Delta-Sigma Data Converters, Theory, Design and Simulation,* IEEE Press, 1996). (For analog applications, such as A/D converters, the digital filter stages and related circuits discussed below will essentially be replaced with their analog equivalents, also described in the publications.)

Filter stages 302a – 302d, each having transfer functions of $1 / (1 - Z^{-1})$, produce the poles and zeros 201 in the right half of the z-plane defined by the positive real axis of FIGURE 2B. The actual locations of the of poles are set by feedforward coefficients C1 – C4. Feedback loops 307a and 307b move the associated zeros along the unit circle (z = 1) from the DC point (Re = 1, Im = 0). Similarly, filter stages 303a and 303b, each having transfer functions of $1 / (1 + Z^{-1})$, and feedforward coefficients C5 and C6, place the poles 202 in the left hand half of the z-plane of FIGURE 2B defined by the negative real axis. Feedback loop 307c moves the associated zeros from the Nyquist point (RE = -1, Im = 0) along the unit circle.

Table 1 gives an exemplary set of coefficients for a typical audio application operating on data with a common input sampling rate of 48 kHz using the topology of FIGURE 3A. The data are upsampled by a factor of 128 such that the Nyquist frequency fs/2 is approximately 3.07 MHz. The resulting noise transfer function is shown in FIGURE 3B, with FIGURE 3C being an expanded view of the noise attenuation in the signal band of the NTF and FIGURE 3D being an expanded view of the noise attenuation at Nyquist. As shown in FIGURES 3B – 3C, the desired two bands of attenuation are produced which will allow splitting of the data from quantizer 300 into odd and even streams into output DAC 108.

TABLE 1

Coefficient	Value for 48 kHz, 128x oversampled audio
C_1	0.472636
C_2	0.213727
C_3	0.0451561
C_4	0.00529628
C_5	0.249534
C_6	0.0537832

An exemplary 8th order feedback delta-sigma modulator 400 which will produce asymmetrical pole-zero sets in the right and left halves of the z-plane is shown in FIGURE 4A. Here, six filter stages 401a - 401f each with transfer functions $1 / (1 - Z^{-1})$ and feedback summers 402a – 402f with respective feedback coefficients C1 - C6 will generate 6 pole-zero pairs in the right half-plane defined by the positive real axis. Two feedback loops 403a and 403b move four of the zeros from the DC (Re = 1, Im = 0) point along the unit circle. Two pole-zero pairs are defined in the left half of the z-plane by filter stages 404a and 404b each having transfer functions $1 / (1 + Z^{-1})$ and feedback summers 405a – 405b with respective feedback coefficients C7 and C8. Feedback loop 406 shifts the two zeros away from the Nyquist point Re = -1, Im = 0.

The outputs from the filter chains respectively formed by filter stages 401a – 401f and 404a – 404b are summed by output summer 407. Quantizer 408 generates the multiple-bit modulator output in this embodiment. The coefficients for an exemplary 48kHz audio sample stream upsampled by a factor of 128 and the feedback topology of FIGURE 4A are provided in Table 2.

TABLE 2

Coefficient	Value for 48 kHz, 128x upsampled audio
C_1	1.79268×10^{-6}
C_2	0.0000567507
C_3	0.000912029
C_4	0.00898768
C_5	0.0646919
C_6	0.262072
C_7	0.187477
C_8	0.46439

FIGURES 4B – 4C respectively show the resulting NTF and expanded views of the noise attenuation in the signal and Nyquist bands.

A third alternative for generating an NTF with multiple attenuation bands is a delta sigma modulator with interleaved loop filter stages. One example is the weighted feedforward modulator 500 shown in FIGURE 5A. In this case, the local noise shaping at Nyquist is characterized by a pair of sets of independent loop filter

stages 501a and 501b interleaved in time by a switch ("SW") or similar circuit 502. Each set of independent filter stages 501a and 501b is represented in FIGURE 5A by a pair of filter stages 503a and 503b, corresponding feedforward stages 504a and 504b with coefficients C_1 and C_2 for setting the local poles, and a feedback loop 505 (with one delay Z^{-1} and gain g^1) and summer 506 for setting the local zeros. (The structure of each set of 501a and 501b may vary from a single filter stage 503 to three or more filter stages 503 and include more than one feedback loop, depending on the desired number and location of the local poles and zeros). The outputs from gain stages 504 of independent loop filter stage sets 501a and 501b are interleaved by a corresponding set of switches 507a and 507b into the modulator output summer 508.

The global (baseband) noise shaping is characterized by a set of shared loop filter stages, in this case three integrator stages 509a – 509c and associated feedforward stages 510a – 510c with respective coefficients C_3 - C_5 into output summer 508. The outputs of stages 501a and 501b are fed into a switch ("SW") 502. The output of SW 502 is, in turn, fed into the first integrator stage 509a. The number of global filter stages may also vary from embodiment to embodiment depending on the desired number and locations of the global pole – zero pairs in the NTF. A feedback loop 511 (during a gain of g1 and a delay Z^{-1}) and summer 512 are shown for moving the global noise shaping zeros on the unit circuit away from the DC point (Re= 1, Im= 0).

A multiple-bit quantizer 513 and a delay element 514 preferably generate the output of modulator 500. The resulting output signal is fed-back to the inverting input of the modulator input summer 514.

By interleaving between independent sets of filter stages 501, each set 501a or 501b is contributing to the input of summer 508 at half the sampling rate. Consequently, the poles and zeros set by filter sets 501a and 501b are translated into the left half-plane around the Nyquist (fs/2) point Re = -1, Im = 0, as generally shown in FIGURE 5B at 520. As with the exemplary embodiments already described, preferably the number of poles and zeros in the right hand half-plane is greater than those in the right hand half-plane. In this example, filter sets 501a and 501b produce two pole-zero pairs around Nyquist and global (shared) filter stages 509a – 509c produce three pole-zero pairs 521 about the DC point.

Figure 6 is an electrical schematic diagram of one embodiment of DAC 108. In this case, a fully differential design is shown. For clarity, a 4-bit DAC operating on 4-bit quantized samples from the DEMs is shown for illustrative purposes, although the quantized sample width will vary from application to application depending on the quantizer used. Generally, while even elements 106a and 106b are sampling charge, odd elements 107a and 107b are dumping charge to opamp 109 and *vice-versa*. Consequently, the current drive capability of opamp 109 is maximized.

In this embodiment, the even samples and their complements (in the differential case) are sent to respective even elements 106a and 106b at the inverting and non-inverting summing nodes of operational amplifier 109, respectively. Even elements 106a for the inverting summing node are shown in further detail, although complementary elements 106b preferably have the same structure. The even elements of blocks 106a and 106b sample charge during Phase 1 (ϕ_1) and dump charge during Phase 2 (ϕ_2). Specifically, switches 605 close at the start of Phase 1 and after a delay (Phase 1 delayed - ϕ_{1D}), input switches 602a – 602d close to sample the corresponding input bits BitA – BitD from even DEM 104 on to the respective input plates of even sampling capacitors 604a – 604d. Switches 603a – 603d and 606 are open during Phase 1. During Phase 2 (ϕ_2), switches 606 initially close and after a delay (Phase 2 delayed - ϕ_{2D}), switches 603a – 603d close to force the charge on the respective input plates of sampling capacitors 604a – 604d to the corresponding summing node of opamp 109. During Phase 2, switches 602a – 602d and 605 are open.

Similarly, the odd samples and their complements are sent to respective odd elements 107a and 107b at the inverting and non-inverting summing nodes of operational amplifier 108. Odd elements 107a for the inverting summing node are shown in further detail, although 107b preferably have the same structure. The odd elements of blocks 107a and 107b sample charge during Phase 2 (ϕ_2) and dump charge during Phase 1 (ϕ_1). Specifically, switches 613 close initially during Phase 2 and after a delay (Phase 2 delayed - ϕ_{2D}), input switches 610a – 610d close to sample the corresponding input bits BitA – BitD from odd DEM 105 on to the respective input plates of odd sampling capacitors 612a – 612d. Switches 611a – 611d and 614 are open during Phase 2. During Phase 1 (ϕ_1), switches 614 initially

close and after a delay (Phase 1 delayed - ϕ_{1D}), switches 611a – 611d close to force the charge on the respective input plates of sampling capacitors 612a – 612d. During Phase 1, switches 610a – 610d and 613 are open.

The principles described above can be extended to instances where more than two attenuation bands in an NTF of a delta-sigma modulator are required. For example, FIGURE 7 illustrates a generalized digital to analog system 700 which operates on N number of phases with N number of DAC elements. System 700 includes a digital data source 701 and a noise shaper 702 generating N number of attenuation bands in its NTF. Noise shaper 702 will be discussed further below.

A splitter 703 partitions the quantized digital data stream from noise shaper 702 into N number of sample streams. DEM 704 then routes the sample streams to N number of switches or similar circuits 704 operating in N number of overlapping phases (ϕ_N). In this embodiment, N number of current-steering DACs 705 convert the sample streams into analog currents which are then summed by summer 706 to produce the final analog output signal.

One advantage of using multiple phases in system 700 is the result of increased smoothness in the analog output signal. Generally, if more phases and current steering DACs exist, then the analog output signal will be smoother. When the input stream is split N times, the mismatch will demodulate the noise from noise shaper 702 into N separate bands. Hence, noise shaper 702 is preferably designed to produce N corresponding noise attenuation bands.

For example, if N = 4 and output from noise shaper 702 is split into four (4) sample streams each at fs/4, then any mismatch between DAC elements 705 will demodulate into the bands fs/4, fs/2 and 3fs/4. Noise shaper 702 therefore should have four corresponding attenuation bands as shown in FIGURE 8A. One possible pole-zero plot that corresponds to these attenuation bands is shown in FIGURE 8B. The pole-zero placement in FIGURE 8B, in one embodiment, is achieved by using the modulator topology of FIGURE 5A modified with four (4) independent filter stages 501a to 501d having outputs four-times interleaved into shared filter stages 503a to 503d. Alternatively, a feedforward or feedback topology having a pair of filter stages with a transfer function of $1 / (1 - Z^{-4})$ and associated feedback loops, which place poles and zeros about Z = 1, -1, j and –j, is also utilized.

In sum, a modulator with multiple noise attenuation bands in the NTF allows the bit stream at the inputs of a DAC, summer, or similar circuit operating in multiple phases, to be split into at least two separate streams. Specifically, the modulator noise potentially demodulated by the switching bit streams between elements with finite mismatch, as well as noise in the signal band, are attenuated in corresponding attenuation bands in the modulator NTF. In turn, the resulting multiple bit streams are converted in separate operating phases to maximize use of conversion circuit elements.

Although the invention has been described with reference to specific embodiments, these descriptions are not meant to be construed in a limiting sense. Various modifications of the disclosed embodiments, as well as alternative embodiments of the invention, will become apparent to persons skilled in the art upon reference to the description of the invention. It should be appreciated by those skilled in the art that the conception and the specific embodiment disclosed may be readily utilized as a basis for modifying or designing other structures for carrying out the same purposes of the present invention. It should also be realized by those skilled in the art that such equivalent constructions do not depart from the spirit and scope of the invention as set forth in the appended claims.

It is therefore, contemplated that the claims will cover any such modifications or embodiments that fall within the true scope of the invention.

WHAT IS CLAIMED IS:

1. A noise shaper comprising a filter system for generating a noise transfer function with first and second attenuation bands.

2. The noise shaper of Claim 1 wherein the first and second attenuation bands include an attenuation band in a signal baseband of the noise transfer function and another attenuation band outside of the signal baseband of the noise transfer function.

3. The noise shaper of Claim 1 wherein first and second attenuation bands correspond to first and second sets of poles and zeros of the filter system.

4. The noise shaper of Claim 3 wherein the first and second sets of poles and zeros comprise first and second sets of poles and zeros spatially separated in a z-plane characterization of the noise transfer function.

5. The noise shaper of Claim 3 wherein the first and second sets of poles and zeros differ in number of poles and zeros in a z-plane characterization of the noise transfer function.

6. The noise shaper of Claim 3 wherein the filter system comprises n number of interleaved filters for generating n number of sets of poles and zeros, where n is an integer greater than 1.

7. The noise shaper of Claim 1 comprising a feed-forward delta-sigma modulator wherein the filter system comprises:

a filter having a first transfer function for characterizing the first attenuation band and receiving a modulator input signal and outputting a first signal for weighted input into a modulator summer and a modulator quantizer at an output of the summer; and

a filter having a second transfer function for characterizing the second attenuation band and receiving an input signal from an output of the quantizer and outputting a second signal for weighted input into the modulator summer and quantizer.

8. The noise shaper of Claim 1 comprising a feed-back delta-sigma modulator wherein:

a filter having a first transfer function for characterizing the first attenuation band and receiving an input signal to the modulator and feed-back from a modulator quantizer and outputting a signal to a modulator summer at an input to

the quantizer; and

a filter having a second transfer function for characterizing the second attenuation band and receiving feedback from the quantizer and outputting a signal to the summer.

9. The noise shaper of Claim 1 wherein the filter system comprises a digital filter system.

10. The noise shaper of Claim 1 wherein the filter system comprises an analog filter system.

11. The noise shaper of Claim 1 wherein the first attenuation band includes DC and the second attenuation band includes the frequency Fs/n, wherein Fs is the sampling frequency and n is an integer greater that one.

12. The noise shaper of Claim 1 wherein the first and second attenuation bands are selected first and second attenuation bands of a plurality of at least two attenuation bands, a sleeted one of the plurality of attenuation bands including DC and other ones of the plurality of attenuation bands including frequencies of Fs/ n • m, wherein Fs is the sampling frequency and m and n are integers, with n greater than one and m less than n.

13. A method of modulating a signal in a delta sigma modulator comprising:

setting a first set of at least one pole-zero pair defining noise attenuation in a first band of a noise transfer function of the modulator; and

setting a second set of at least one pole-zero pair defining noise attenuation in at least one second band in the noise transfer function of the modulator, the first and second numbers of pole-zero pairs selected to produce a difference in noise attenuation between the first and second bands in the noise transfer function.

14. The method of Claim 13 wherein said steps of setting the first and second sets of at least one pole-zero pair comprise the steps of setting first and second sets of at least one pole-zero pair rotated with respects to each other about the origin of a z-plane characterization of the noise transfer function of the modulator.

15. The method of Claim 13 wherein said steps of setting the first and second sets of at least one pole-zero pair comprise the steps of setting first and second sets of unequal numbers of pole-zero pairs.

16. The method of Claim 13 wherein said steps of setting the first and sets of at least one pole-zero pair comprise the steps of placing the pole-zero pairs about the DC and Nyquist points of a z-plane characterization of the noise transfer function of the modulator.

17. The method of Claim 13 wherein said steps of setting first number of pole-zero pairs comprise the steps of placing about the DC point on a unit circle of a z-plane characterization of the noise transfer function of the delta sigma modulator and the second number of pole-zero pairs comprises n number of sets of pole-zero pairs placed at points about the unit circle in the z-plane characterization of the noise transfer function of the delta sigma modulator spaced from the first number of pole-zero pairs to define n number of attenuation bands in the noise transfer function.

18. The method of Claim 13 wherein said step of setting the second set of at least one pole-zero pair comprises the substep of interleaving first and second filter stages.

19. The method of Claim 13 further comprising the step of selecting a modulator topology of a selected number of filter stages wherein:

said step of setting the first set of at least one pole-zero pair comprises the substep of selecting at least one filter stage having a first transfer function; and

said step of setting the second set of at least one pole-zero pair comprises the substep of selecting at least one filter stage having a second transfer function.

20. The method of Claim 13 wherein the modulator comprises a digital delta-sigma modulator.

21. The method Claim 13 wherein the modulator comprises an analog delta-sigma modulator.

22. A data converter comprising:

a delta-sigma modulator having a noise transfer function with a plurality of noise attenuation bands including a first noise attenuation band for attenuating noise in a converter output signal baseband and at least one second noise attenuation band;

circuitry for splitting the output signal from the modulator into a plurality of intermediate signals;

a plurality of interleaved data conversion elements each for converting a

corresponding one of the intermediate signals from a first form to a second form; and

a summer for summing output signals from the conversion elements into the converter output signal, the second noise attenuation band of the modulator characterized to attenuate noise output from the modulator and demodulated by mismatch between the interleaved conversion elements.

23. The data converter of Claim 22 wherein the circuitry for splitting splits the output signal into n number of intermediate signals for conversion by n number of interleaved conversion elements and the at least one second noise attenuation band comprises n number of attenuation bands in the noise transfer function of the modulator.

24. The data converter of Claim 22 wherein the interleaved data conversion elements comprise a plurality of switched-capacitor elements operating in interleaved operating phases.

25. The data converter of Claim 22 wherein the interleaved data conversion elements comprise a plurality of current steering elements operating in interleaved operating phases.

26. The data converter of Claim 22 wherein the first form is digital and the second form is analog.

27. The data converter of Claim 22 wherein the first form is analog and the second form is analog.

28. The data converter of Claim 22 wherein a difference in noise attenuation levels between the first noise attenuation band and the at least one second noise attenuation bands is selected as a function of a degree of the mismatch between the interleaved conversion elements.

29. The data converter of Claim 22 wherein the delta-sigma modulator produces at least two sets of pole-zero pairs, each set differing in number and location of the pole-zero pairs on the z-plane.

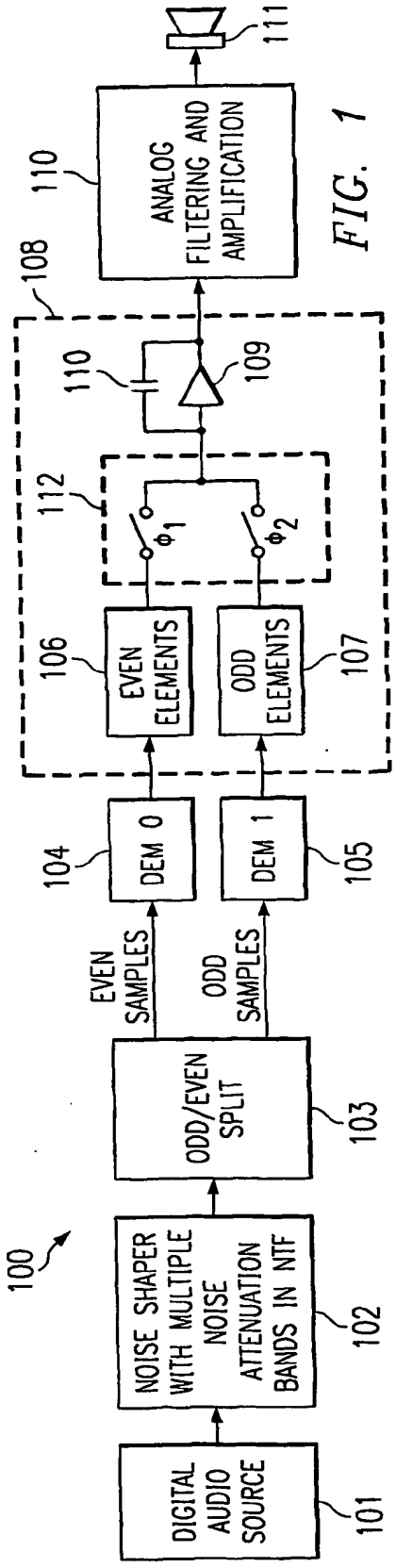


FIG. 1

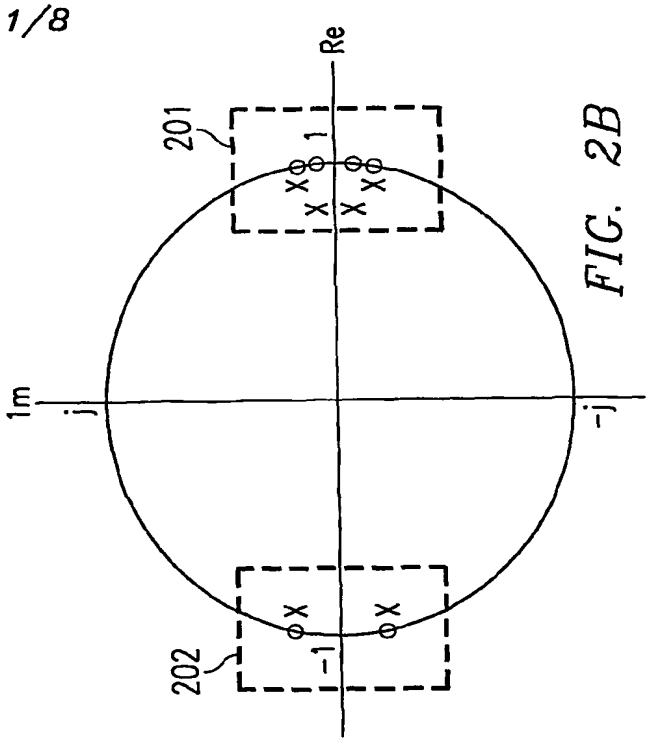


FIG. 2B

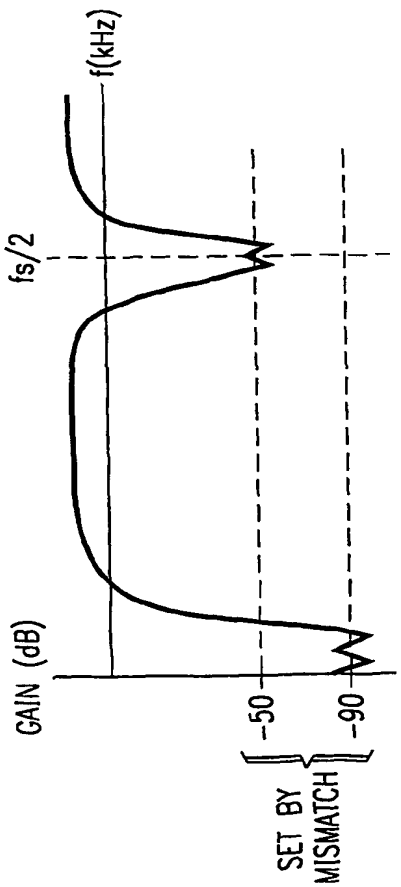


FIG. 2A

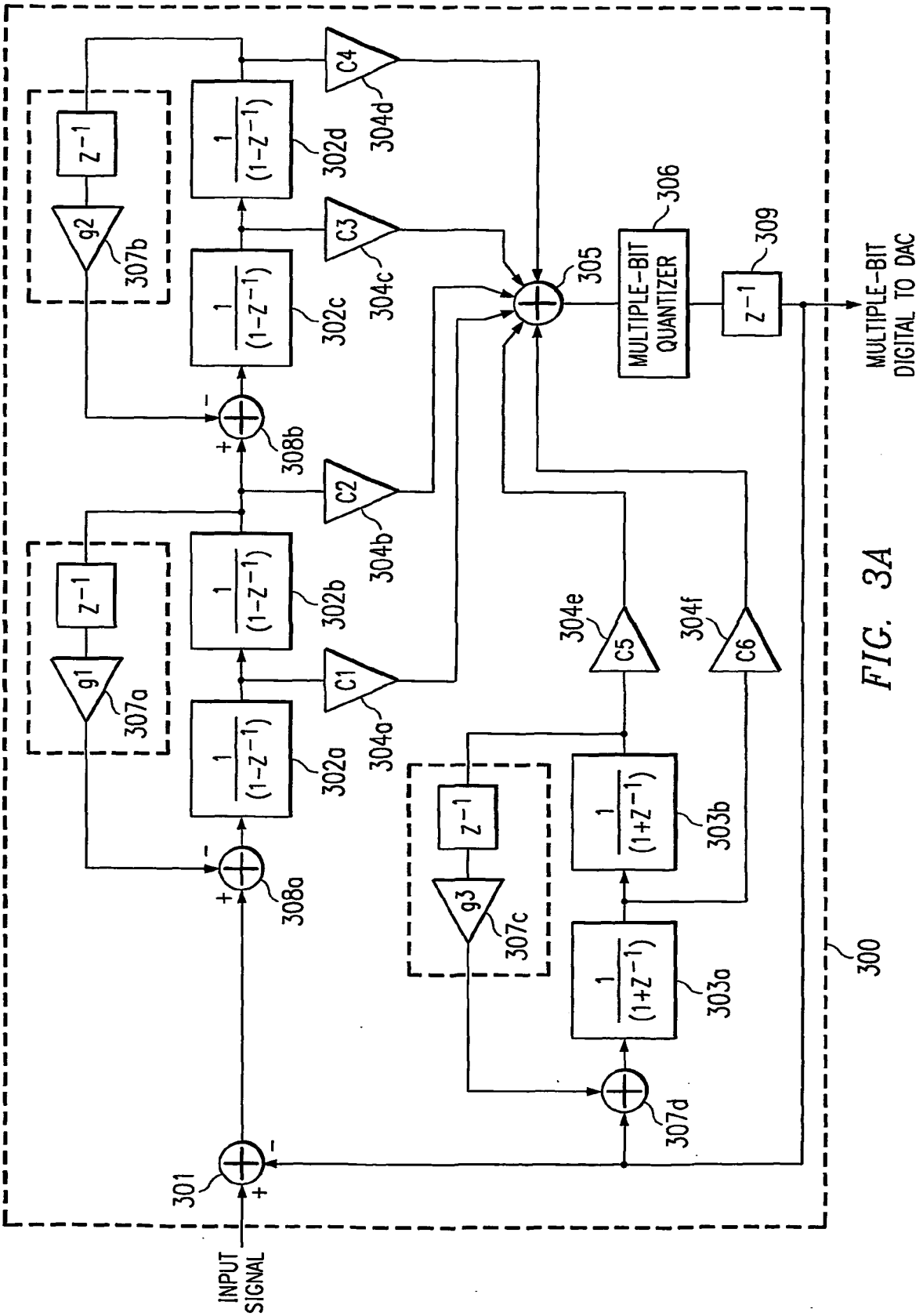


FIG. 3A

FIG. 3B

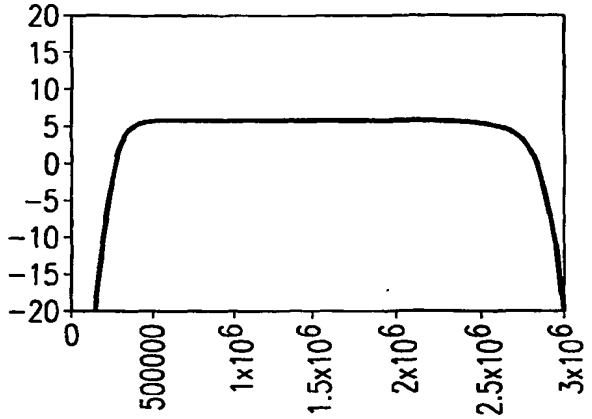


FIG. 3C

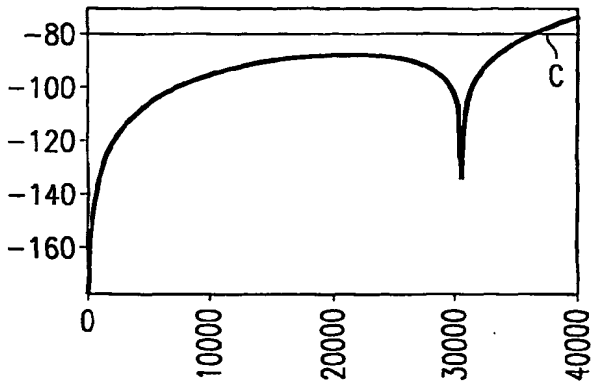


FIG. 3D

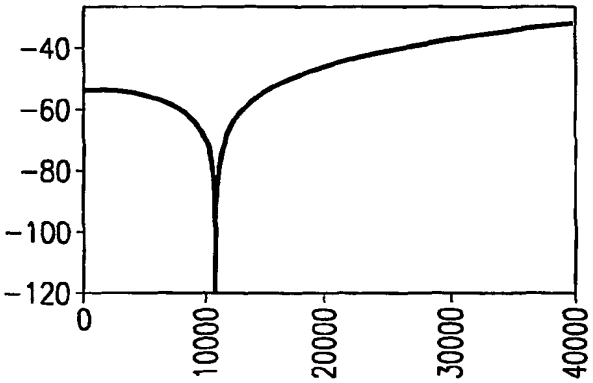


FIG. 3E

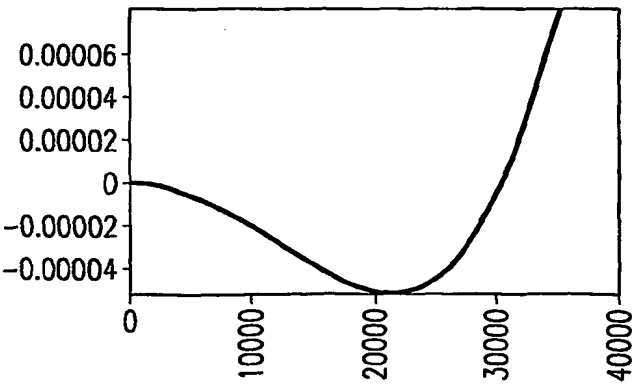
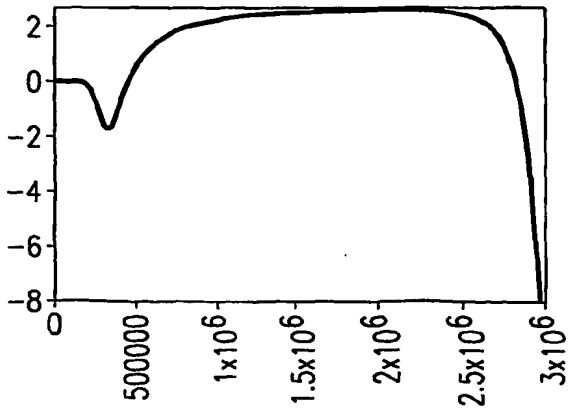


FIG. 3F



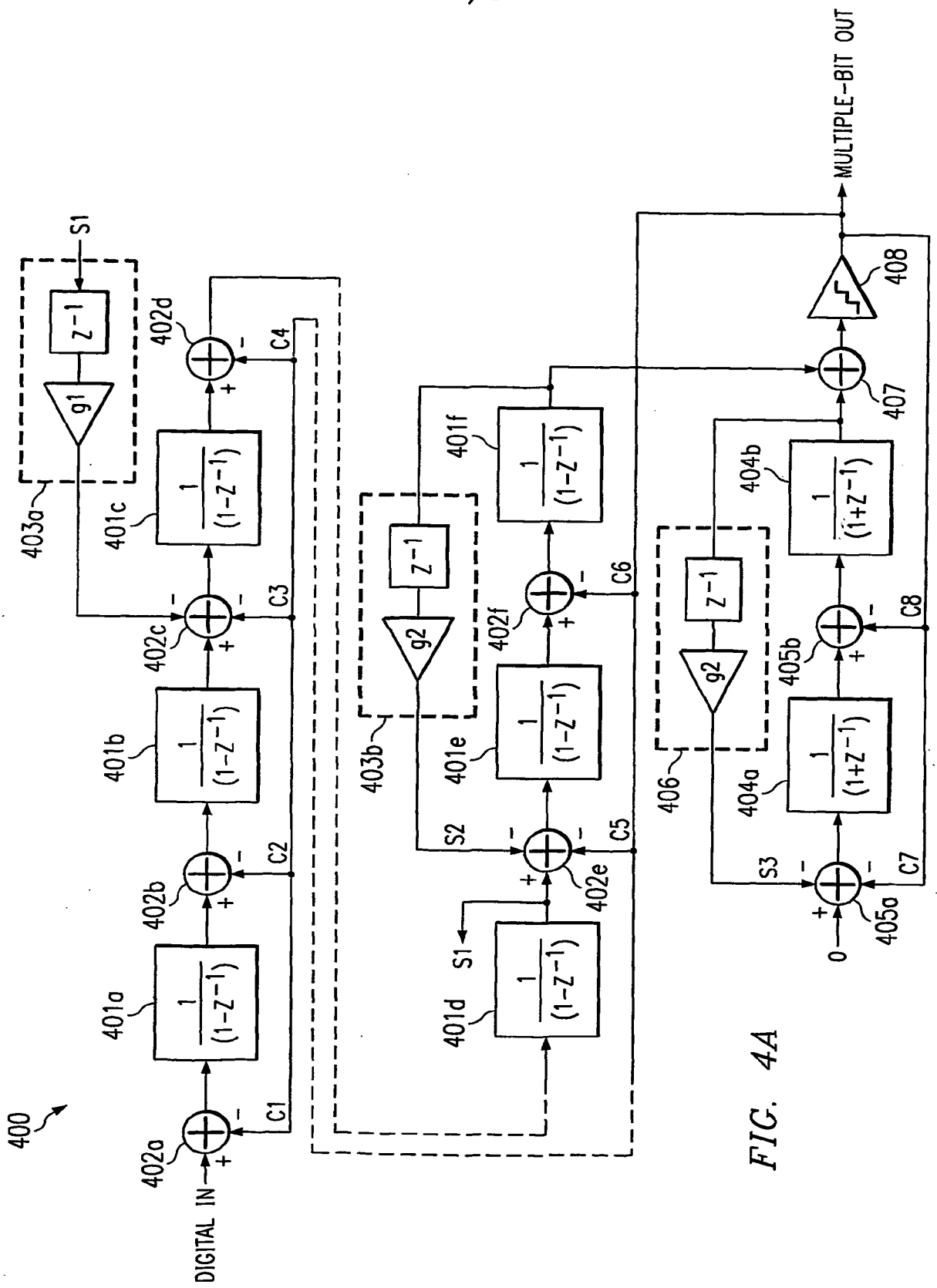


FIG. 4A

FIG. 4B

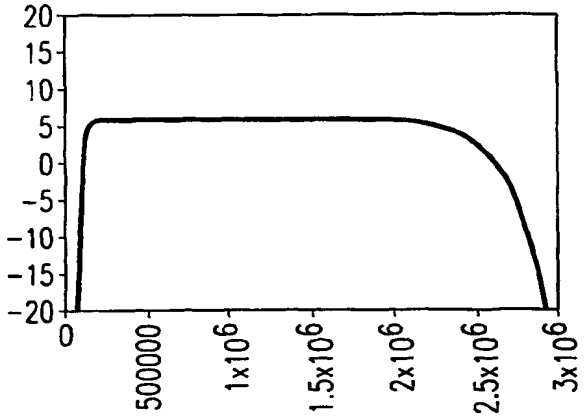


FIG. 4C

FIG. 4D

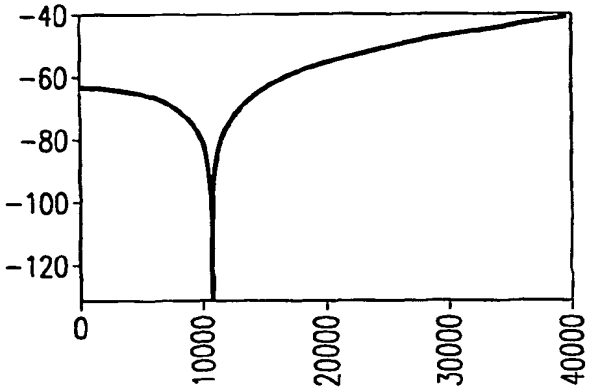


FIG. 4E

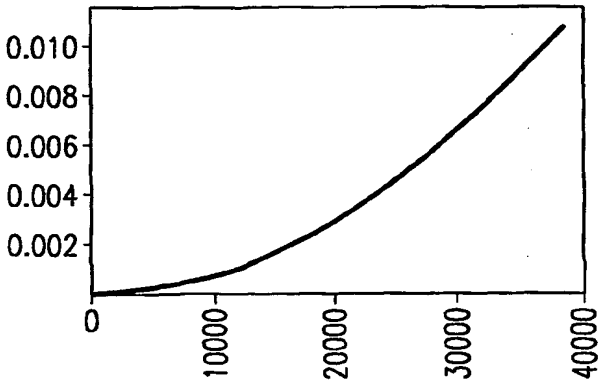
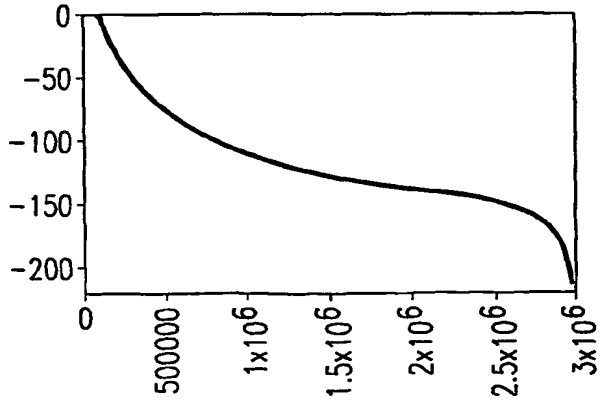


FIG. 4F



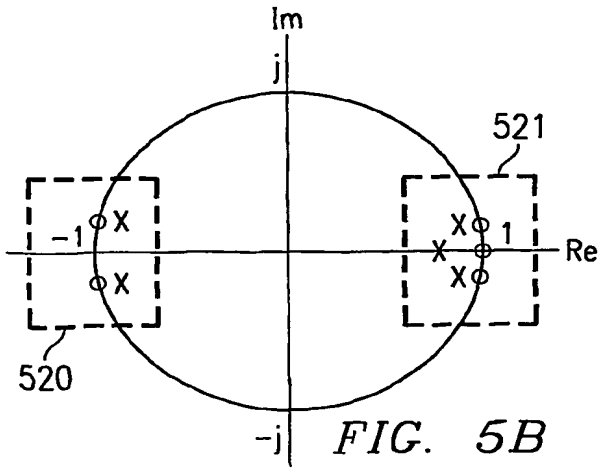


FIG. 5B

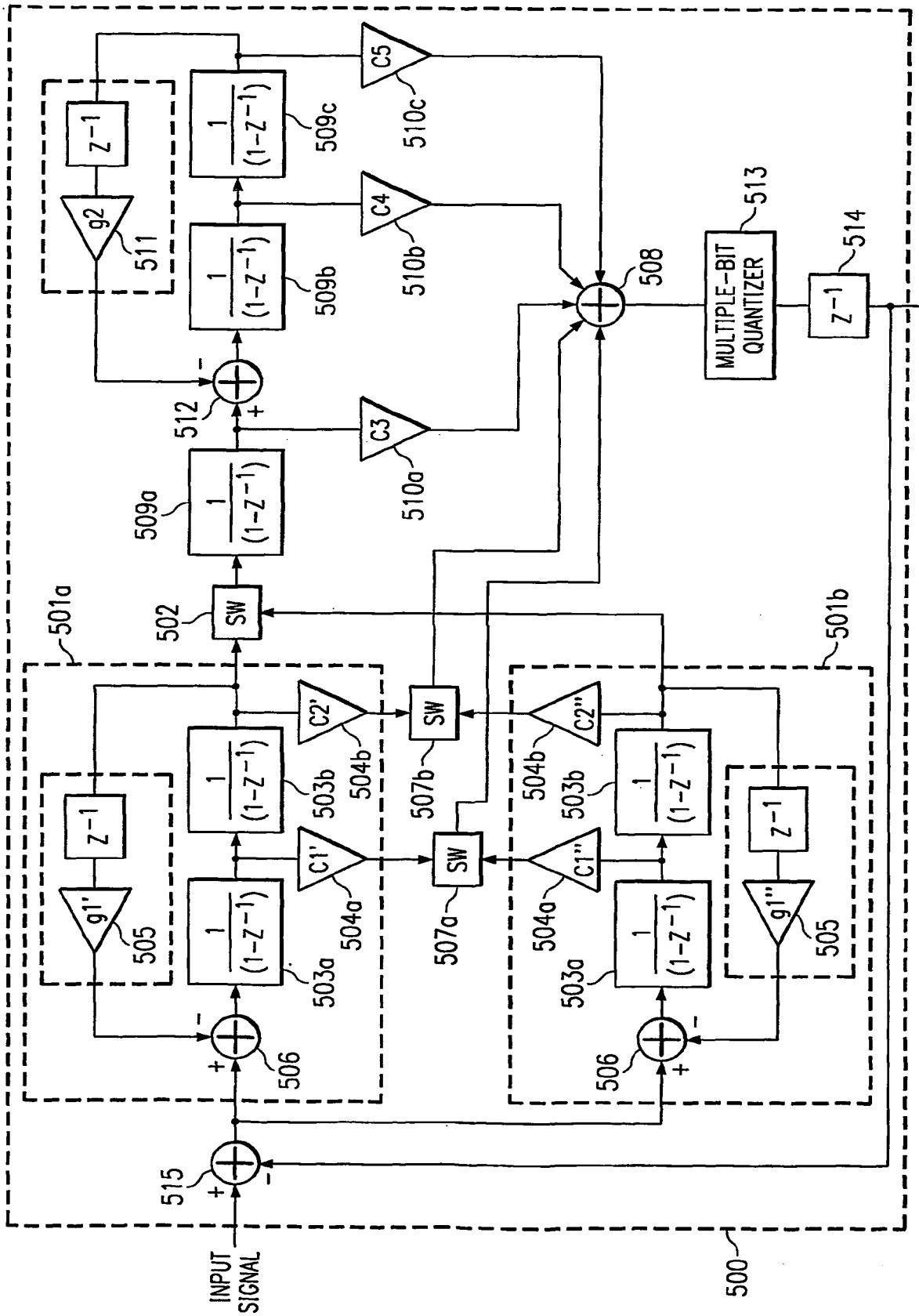
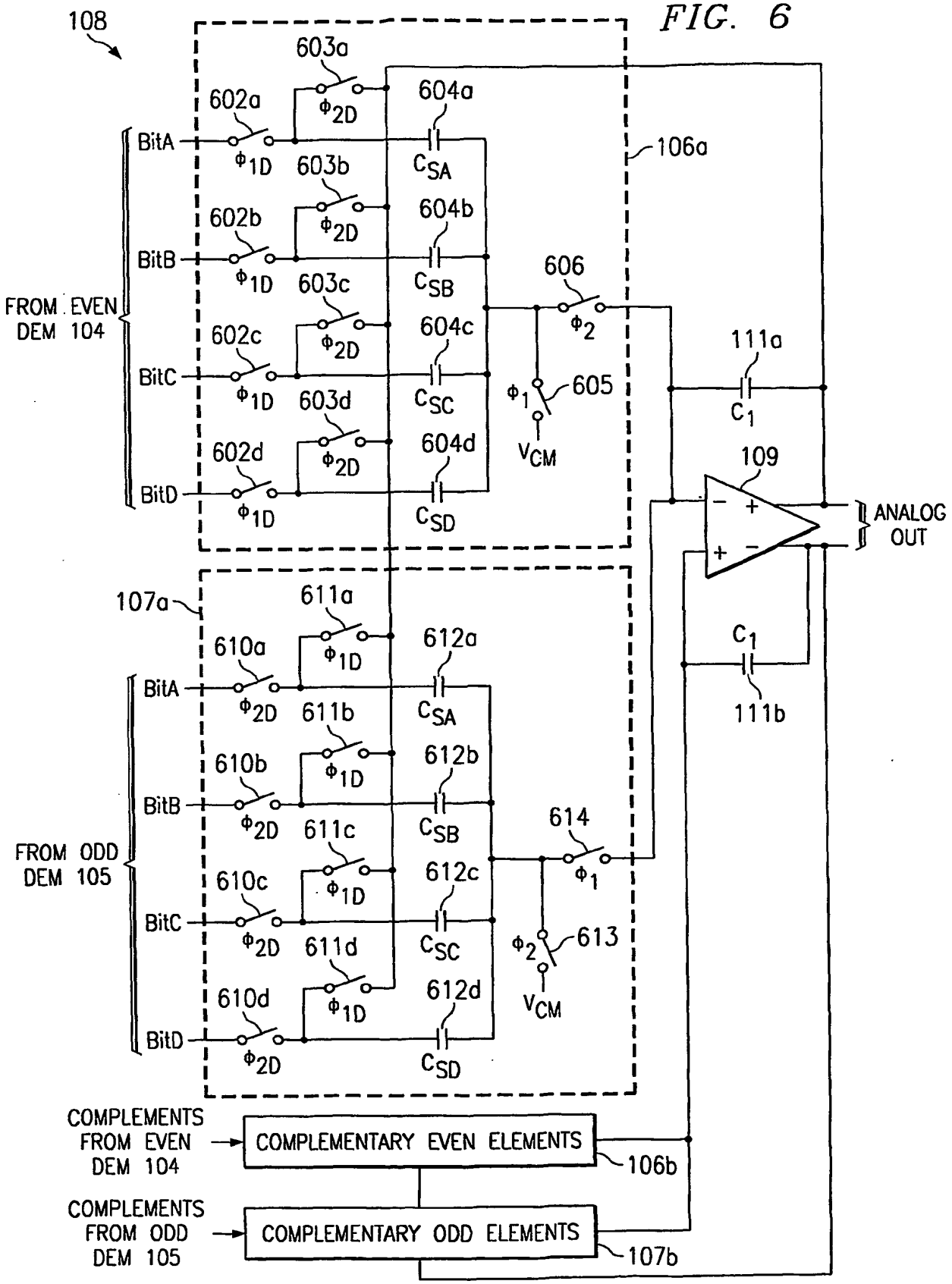

INPUT SIGNAL
MULTIPLE-BIT DIGITAL TO DAC
MULTIPLE-BIT QUANTIZER
SW
500
501a
501b
502
503a
503b
504a
504b
505
506
507a
507b
508
509a
509b
509c
510a
510b
510c
511
512
513
514
515
C1'
C1''
C2'
C2''
C3
C4
C5
g1'
g1''
g2
Z-1
1/(1-Z-1)

FIG. 5A

FIG. 6


108
603a
602a
604a
BitA
Φ_{1D}
Φ_{2D}
C_{SA}
106a
603b
602b
604b
BitB
C_{SB}
606
603c
602c
604c
FROM EVEN DEM 104
BitC
C_{SC}
Φ_2
111a
Φ_1
605
V_{CM}
C_1
603d
602d
604d
BitD
C_{SD}
109
ANALOG OUT
107a
611a
610a
612a
611b
610b
612b
614
FROM ODD DEM 105
611c
610c
612c
613
611d
610d
612d
COMPLEMENTS FROM EVEN DEM 104
COMPLEMENTARY EVEN ELEMENTS
106b
COMPLEMENTS FROM ODD DEM 105
COMPLEMENTARY ODD ELEMENTS
107b

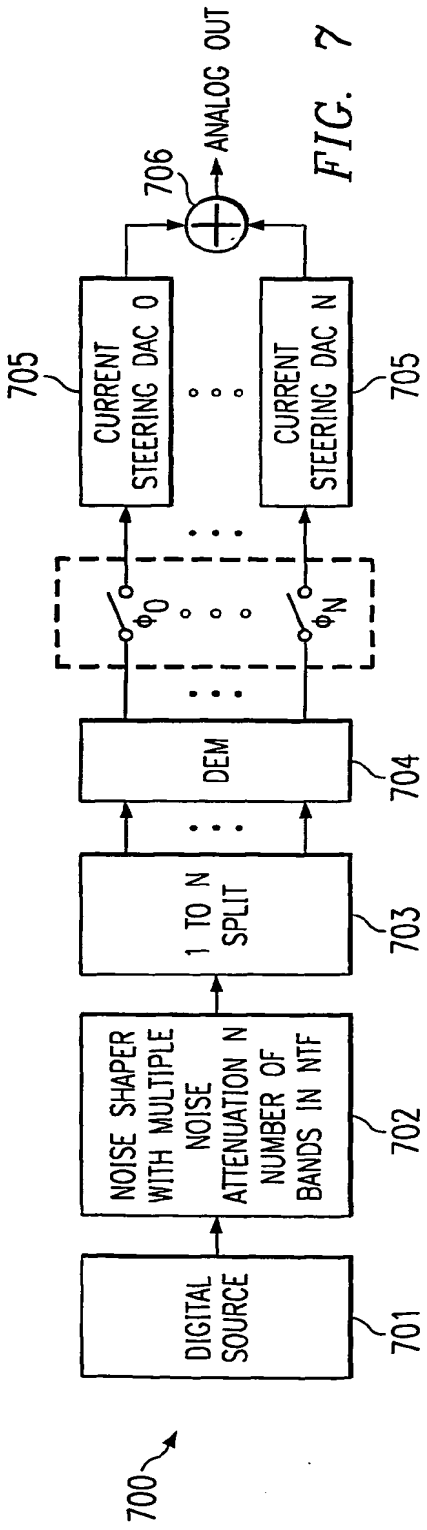


FIG. 7

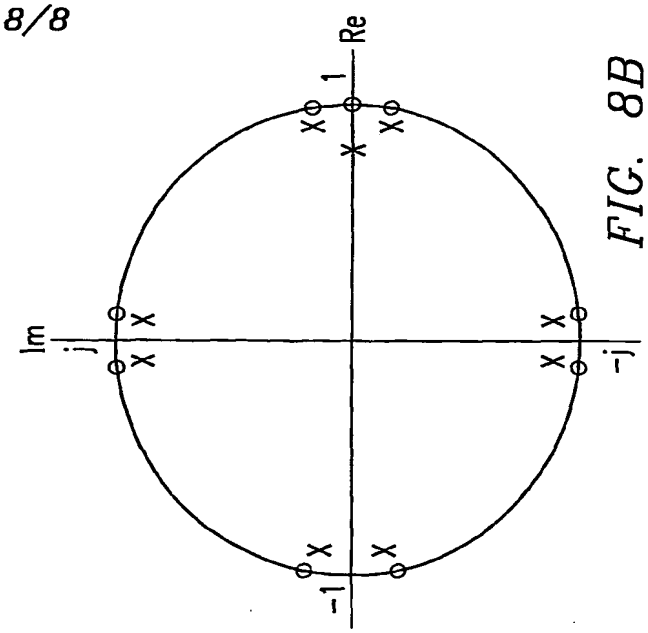


FIG. 8B

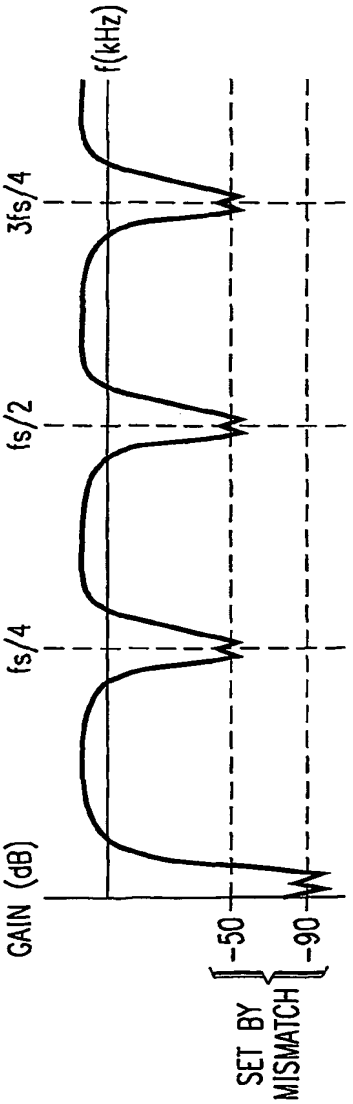


FIG. 8A

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US03/11777

A. CLASSIFICATION OF SUBJECT MATTER

IPC(7) :HO3M 3/00; HO3M 1/66
US CL :341/143

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 341/143, 144

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EAST

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5,392,042 A (Pellon) 21 February 1995, col. 15, lines 1-59 and col. 4, line 49 to col. 5, line 55.	1, 3-4, 6-10, 13, 16-21
E, A	US 6,414,566 B1 (Atokawa) 02 July 2002, Fig. 1, abstract.	1, 3-4, 6-10, 13, 16-21
E, A, P	US 6,472,953 B1 (SAKURAGAWA et al.) 29 October 2002, see claims.	1, 3, 4-6

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search 25 MAY 2003	Date of mailing of the international search report 06 OCT 2003
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 305-3230	Authorized officer PEGUY JEANPIERRE Diane Smith Telephone No. (703) 308-1968

Form PCT/ISA/210 (second sheet) (July 1998)★